

Closed Loop Software Control of the MIDE X Power System

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Abstract—MIDE X (Medium Class Explorer) is NASA's medium class series of scientific spacecraft. The MIDE X power system was designed to be adaptable to multiple missions, and will be used on the Microwave Anisotropy Probe (MAP), Earth Orbiter-1 (EO-1) and, with modifications, on the Imager for Magnetopause-to-Aurora Global Exploration (IMAGE) spacecraft. The power system design achieves its flexibility in part by containing mission unique modifications in software and firmware. Historically at Goddard Space Flight Center, the power system control loop was closed with analog hardware. In the MIDE X power system design, the outer system control loop is implemented with microprocessor based software. While the ease of adjustability in software allows the design to accommodate Low Earth Orbit (LEO), GEO (Geosynchronous Orbit) or Libration point full sun missions, as well as any solar cell or battery technology, digital control poses a number of challenges.

The power system is a direct energy transfer (DET) topology with the solar array and battery connected directly to the bus. Solar array power is controlled by seven digitally switched, nondissipating shunts, two pulse width

modulated (PWM) segments and one unswitched segment. The inner control loop of the PWM converter is closed with analog electronics. However, the system control loop, including the battery charge control, is accomplished digitally. The microprocessor monitors the state of the system, does fault detection and correction, performs the battery charge control calculations, controls the solar array shunts and sends a drive signal to the PWM converter.

This paper describes the performance and stability of the inner analog and outer digital control loops. The system was modeled and its system response was analyzed in each operating mode—each of two constant current (CC) modes and one voltage/temperature (V/T) mode. The analysis was verified by measurements in the lab. The analysis and measurements showed that the solar array PWM input filter and the software algorithm have significant influence on the system operating range and system response. A number of challenges were encountered in implementing Goddard's first spacecraft to use a digital power system control. These challenges and the solutions are addressed.

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1. INTRODUCTION

The MIDEX power system was developed at NASA Goddard Space Flight Center as a generic power system, capable of adapting to a number of missions in the range from 250 to 400 Watt orbital average mission load. This design will be used for the EO1 and MAP spacecraft and will be modified for use on the IMAGE spacecraft. In designing the MIDEX power system, the following design goals were emphasized: reduced cost, adaptability to other missions, maximal use of standard off-the-shelf components and minimal integration and test (I&T) time with the spacecraft. The design is flexible enough to accommodate multiple solar array segment layouts and multiple battery technologies. Other features of the power system are: the elimination of relays and fuses in favor of solid state, resettable circuit breakers, the reduction of board space with the use of surface mount components, and the ease of manufacture resulting in the elimination of the internal box harness.

2. RECENT HISTORY OF POWER SYSTEMS AT GSFC

In an effort to address the NASA's goal for faster, better, cheaper spacecraft, the MIDEX spacecraft architecture emerged. The key features of this spacecraft architecture are the ability to accommodate multiple missions, reduced cost and standardized interfaces[1]. In conjunction with this effort, this modular power system design was developed. The system can be adapted easily to a number of missions in the 250 Watt to 400 Watt load range by adding the appropriate modules. In using this modular, flexible system the expense of non-recurring engineering design work can be avoided and resources can be refocused toward the critical science requirements, rather than the spacecraft infrastructure. This power system is an attempt to meet that challenge.

Historically at Goddard Space Flight Center (GSFC), the power system control loop was closed with analog circuitry. The MIDEX power system is the first GSFC use of power system control closed in software. The power bus architecture (Figure 1a) consists of 7 digitally switched, non-dissipating, full shunts, in the form of solid state switches, to do the coarse adjustment in solar array power. Fine adjustments are made with the 2 solar array segments connected to the bus through a pulse width modulated (PWM) converter. As shown in Figure 2, drive signals for the PWM and for the digital shunts are calculated by the software.

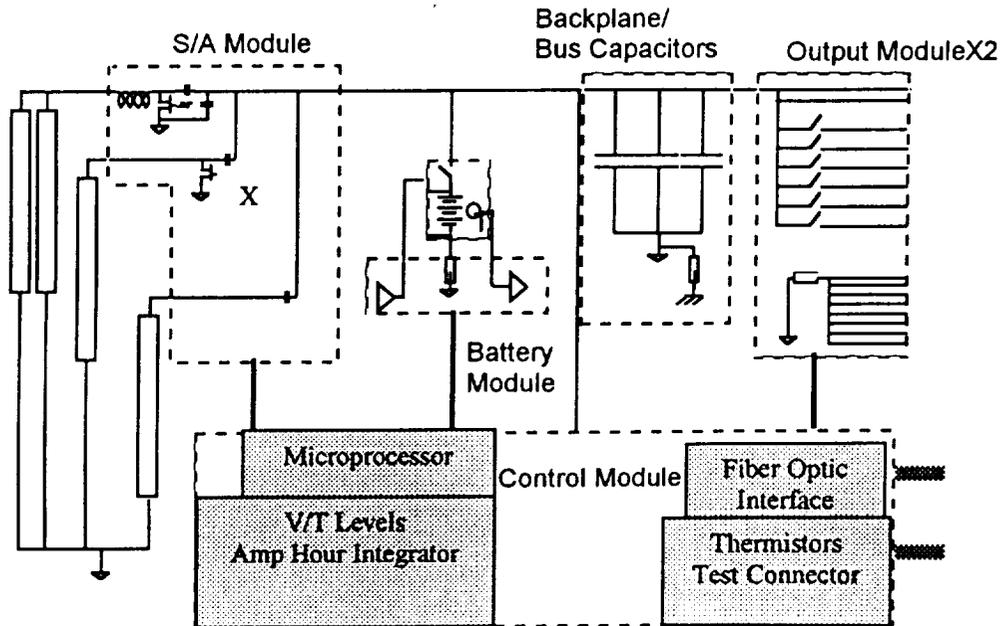


Figure 1a: Functional Block Diagram of the MIDEX Power System Electronics

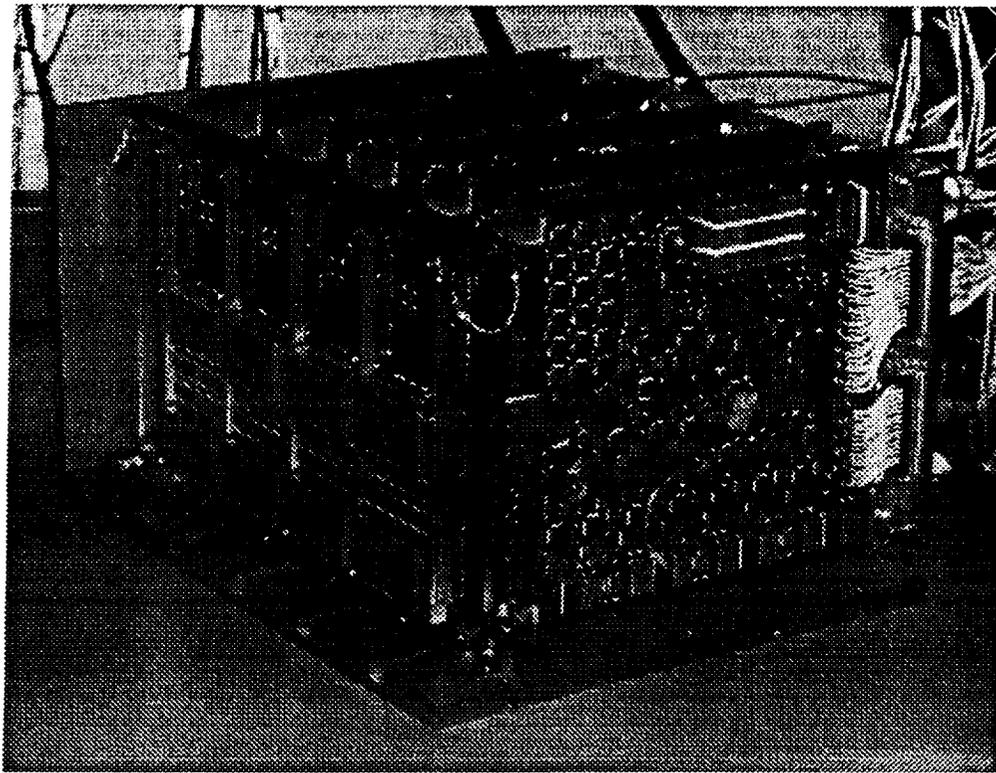


Figure 1b: Photograph of Power System Electronics Hardware

Battery charge control is also calculated by the system code. The temperature compensated voltage-temperature (V/T) levels and ampere hour integration constants are stored as tables. These calibration constants can be changed to do charge control on other battery technologies and sizes. All critical functions have hardware backups in the case of a processor failure.

With this partial digitally controlled power system, the ease of adapting the control to various battery and solar array types and sizes is gained, and the control loop compensation can be tuned to differing load profiles and transients expected. However, a number of challenges are presented with the digital control that are described and addressed here. This paper will describe the MIDEX power system as applied to the MAP power system, including the battery and solar array.

3. THE POWER SYSTEM OF THE MAP SPACECRAFT

The Microwave Anisotropy Probe (MAP) is a NASA science satellite designed to measure temperature gradients in the cosmic background radiation. The MAP will use a lunar gravity assist to achieve its orbit around the L2 libration point and will take scans for the length of the 2 year mission.

The power requirements for this satellite are 325 Watt-hours from a combination of battery and solar array power during launch, 420W for a maximum of 120 minutes during maneuvers and 400W continuously while in orbit. The major power loads are three reaction wheels (each having 125W peak power, 17W average), which will turn on during the launch sequence and a 150W microwave radiometer which will be operated while the satellite is in orbit. Some of the other critical loads are the spacecraft's computational hub, the Command and Data Handling unit (C&DH), the transponder which is the communications link to the ground, and the Attitude Control Electronics (ACE) which performs the spacecraft navigation and attitude control. Power is supplied by 22 Nickel Hydrogen battery cells for the launch phase and maneuvers. The solar array is composed of 12 segments of GaAs solar cells.

The Power System Hardware

The battery and solar arrays are connected directly to the power bus for which a voltage of 21-35V is maintained. The electronics that regulate the solar array power and perform the battery charging are located in the Power System Electronics (PSE) unit. The solar array module in the PSE can be customized through internal jumpers to

accommodate different numbers of solar array segments, each with a conservative derating of 2.5 Amps each. For MAP, the card is jumpered for 12 array segments. Nine of the solar array segments connect to 7 digitally switched, solid state shunts and 3 segments connect to the PWM converter. The shunts, surface mount Field Effect Transistors (FET), are switched according to the power needs of the battery and loads. For stability and fine tuning, 3 solar array segments (5.6 Amps for the MAP array) are connected to the bus through a switchmode regulator, which is continuously controlled. (See Figure 1.)

The control of this regulator ensures that bus voltage transient and noise specifications are met. These specifications state that bus voltage swings in response to a load change cannot exceed 3V. The maximum expected load change is 150W. Power bus noise is limited to 0.5V peak-to-peak (p-p) and common mode noise is constrained to 100mVp-p. Another requirement levied on the power system limits bus voltage fluctuations to less than 0.5Vp-p with 10Wp-p of noise imposed on the bus. This accounts for the maximum expected power variations of the reaction wheels in the L2 orbit. The reaction wheels keep the spacecraft spinning for the instrument to perform its scans. The transfer of momentum among the reaction wheels produces a sinusoidal oscillation on the power bus.

Each of these performance specifications has been modeled for predicted system behavior and measured in the lab with the PSE engineering unit. The system step response follows under various conditions. Appendix A describes the hardware model of the solar array pulse width modulator hardware and the efforts undertaken to choose the simplest and most robust design for the compensation.

The battery is connected directly to the bus and the commanded battery current is calculated in software based on the state of charge (SOC) and the voltage/temperature (V/T) ratio of the cells. The temperature compensated voltage levels and amp hour integration constants are stored as tables in memory. An overview of the control system operation, including the solar array power regulation and battery charge control is given in the following section.

The Detailed Power System Electronics Design—The Power System Electronics (PSE) is composed of modules or printed circuit board (PCB) assemblies that can be added or removed depending on the mission requirements. Following is a list of the module names in the PSE:

- Solar Array Module (SAM)
- Battery Module
- Output Module
- Control Module
- Low Voltage Power Converter Module (LVPC)
- Backplane

The Solar Array Module houses all the nondissipating or digital solar array shunts as well as the PWM circuit and the overvoltage bus protection. For power sources greater than 750 Watts, additional SAMs are needed. Up to 3 SAMs can be added in the present backplane design. One Battery Module can accommodate any battery technology and battery sizes up to 50 Amp-hours. Missions flying multiple batteries will require an additional module that can be added to the present system design without additional non-recurring engineering. Battery voltage, current, temperature, pressure are measured and battery relay commands are sent to this module. The Output Module does the power switching and distribution by supplying overcurrent protected services to the spacecraft subsystems and instrument. The MAP and EO-1missions each use 2 Output Modules for a total of 12 switched services and 4 unswitched services. Here solid state overcurrent protection is provided without fuses. The power system computer and Analog to Digital converters (A/D) reside on the Control module. The battery charge control and solar array PWM control signals are generated by the system code running on the radiation-hardened microprocessor. The LVPC delivers the conditioned power to the PSE internal box electronics and provides additional switched and overcurrent protected primary power services for thermal control on the spacecraft. The Backplane connects the modules together, provides terminations for the digital signal lines and conditions the power bus with multichip ceramic capacitors.

Simply stated, the microprocessor accomplishes system control by monitoring the battery condition and solar array regulator PWM status and by adjusting control signals to the PWM and digital solar array shunts accordingly. The system operates by maintaining a regulated battery current throughout changes in loads. An increased power demand by the loads will result in additional solar array power made available by opening a digital shunt (turning the shunt switch off) or by adjusting the drive signal to the PWM converter. A more detailed description of this operation is presented below.

Power System Software Design

In order to make the software control adaptable to other missions, the code was designed to be table driven. All calibration constants and algorithm coefficients are saved in tables that can be modified on orbit by ground command. A list of some of the adjustable parameters is given below:

- Battery Size
- Amp Hour Integrator Gain
- Battery Recharge Ratio
- Battery Constant Current Charge Levels
- Battery Trickle Charge Threshold
- Battery Voltage Temperature Curves
- Solar Array Segment Number
- Solar Array Segment Size
- Other Analog Telemetry Calibration Curves

A block diagram of the power bus controllers in the power system electronics (PSE) is shown in Figure 2. The system has several embedded loops. The logic for the main outer loop is implemented in software on UTMIC's UT69R000 microprocessor and provides autonomous control of the power system.

The software control consists of 2 loops—one operating at a 500 millisecond (msec) update rate and one at 4 msec. The 500 msec loop does the V/T control. Battery temperature is sampled every 500 msec and a desired voltage for proper V/T control of the battery is calculated. The 4 msec loop performs the amp hour integration, calculates the PWM

control signal and switches the digital solar array shunts as needed. Battery voltage and current as well as the duty cycle of the converter are sampled by the microprocessor every 4 milliseconds. The desired battery current is calculated from the state of charge and V/T levels.

The microprocessor also controls the state of the 7 digital solar array shunts depending on the percent duty cycle, %D, of the PWM signal of the converter. A duty cycle greater than 90% indicates that the power load demand is high relative to the supply and causes the digital controller to open one of the solar array shunts, thus increasing the power available to the bus. Likewise a solar array shunt closes when the duty cycle falls below 10%. This procedure is also executed every 4msec, if needed.

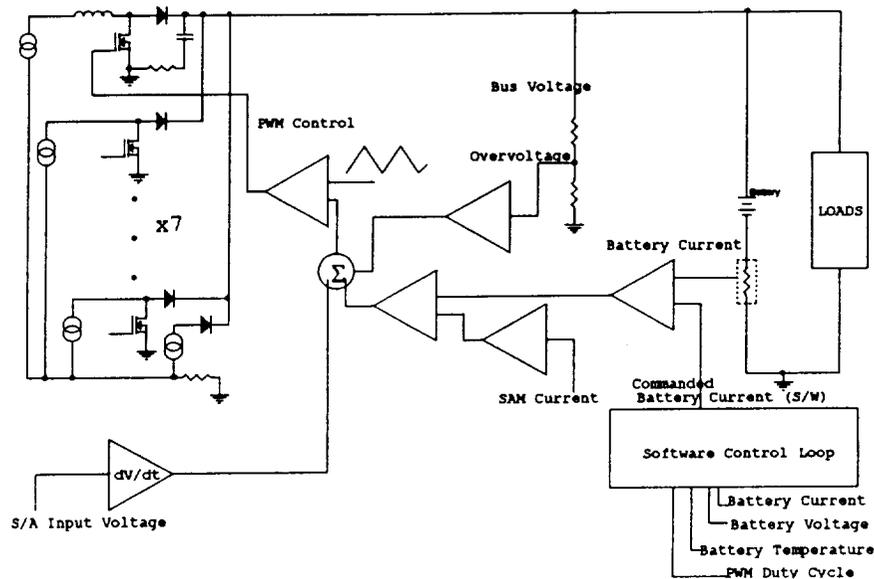


Figure 2: Block Diagram of the Power Bus Controllers in the PSE.

Table 1: MAP Power System Requirements and Test Results

Requirement	Test Results	Comments
Bus V with Load Transients < 3V	0.5V	Instrument, 150W
Bus Noise < 0.5Vp-p	14mV	Switching spikes, 125kHz
Spin Noise < 0.5Vp-p w/10W load var.	30mV	
Common Mode Noise < 100mVp-p	60mV	

Test Results and Software Control

A summary of the major performance test results is shown in Table 1 along with the corresponding specification. The MAP power system meets all required limits with some margin.

Testing of the PSE revealed that an appropriately designed input filter has a major influence on the stability of the converter. The modeling described in Appendix A supports these test results. Other tests indicated that signal bandwidth and the algorithm used to calculate the drive signal to the PWM was critical to system response. By adjusting the various gain and offset constants loaded in the

table-driven code, we could fashion a response to load transients appropriate for our system parameters. In other words, by tweaking the gain of one of the expressions, we can influence the system response. Figure 3 illustrates the system response with the gain of the first control factor set to 0.5. Figure 4 is the system step response with the control factor gain set to 0.1. The system overcorrects when the gain of this control factor is set too high. The optimal value was found to be 0.1. Both figures illustrate response to a 5 Amp load change imposed at time $t=200\text{msec}$ and to 10 Watts of noise imposed continuously. From zero to 25msec, the system exits eclipse and charges the battery. At time $t=450\text{msec}$ the battery is fully charged and the microprocessor commands the system to go into battery trickle charge mode.

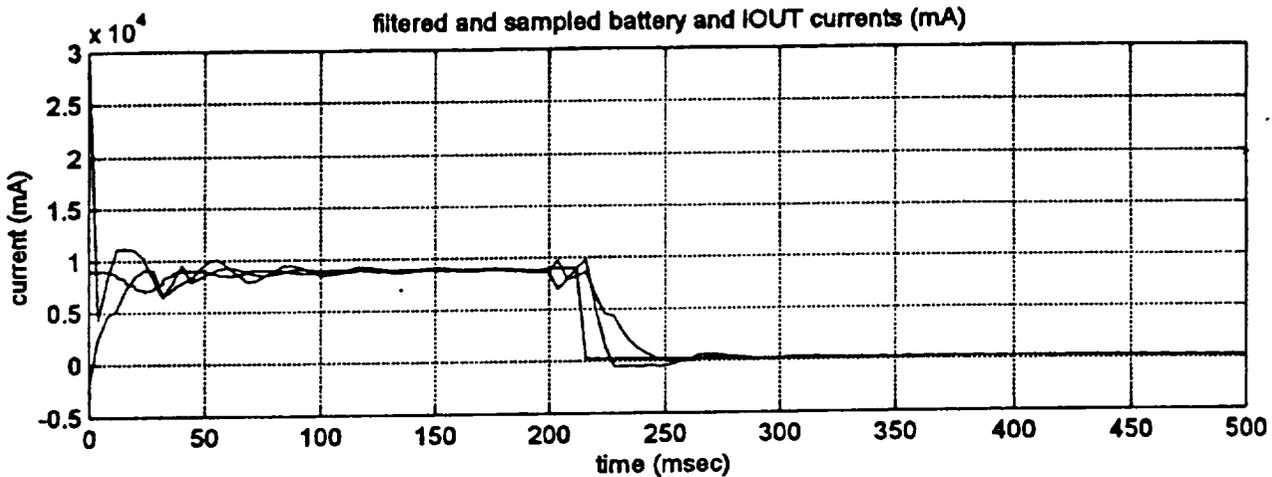


Figure 3: System Step Response with Control Factor Gain Set to 0.5.

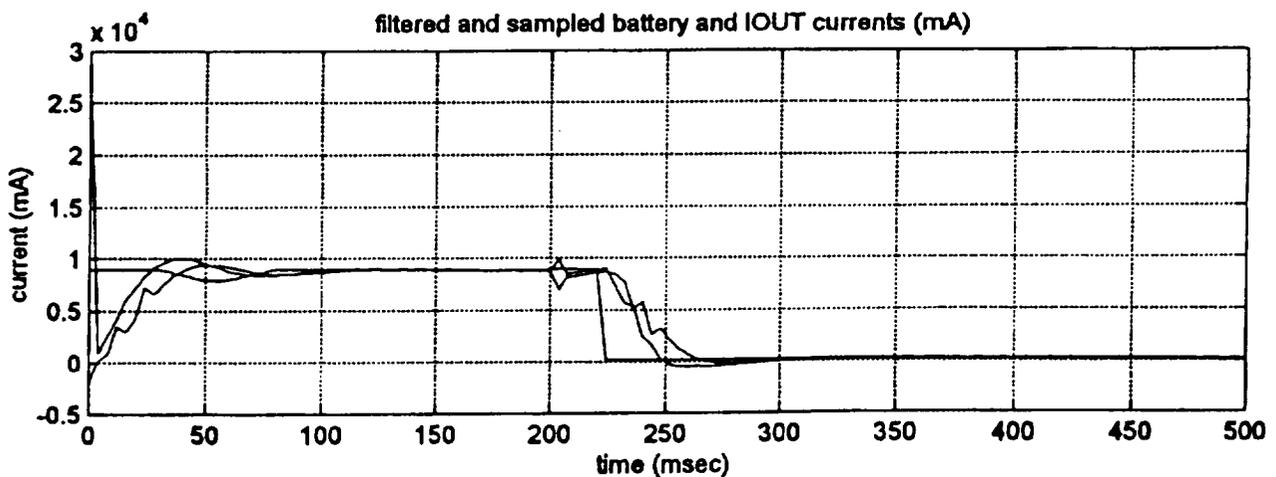


Figure 4: System Step Response with Control Factor Gain Set to 0.1.

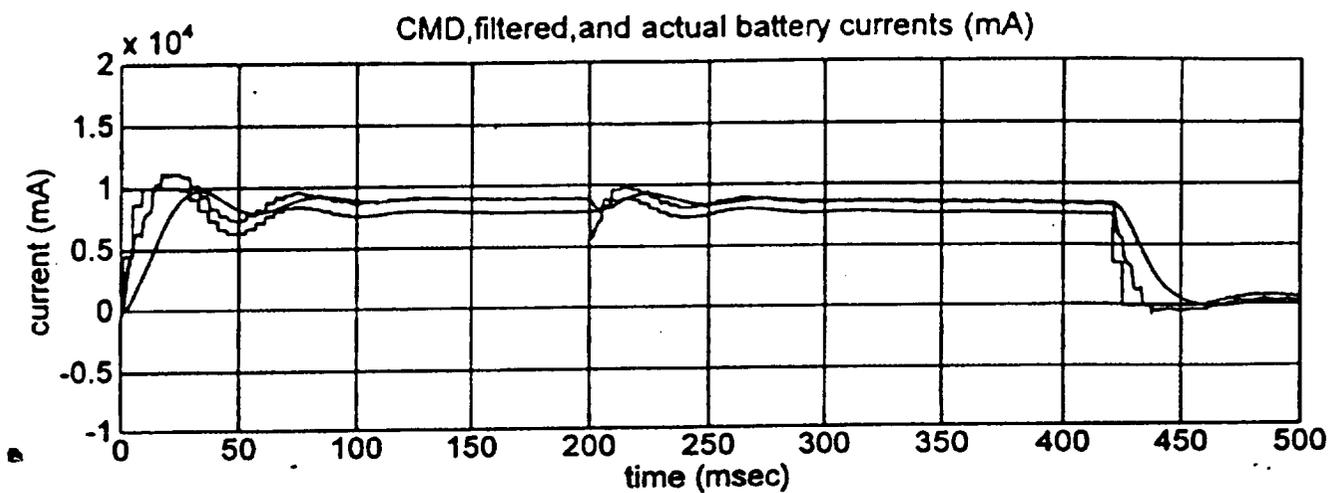


Figure 5: Low Bandwidth System Response to a 5 Amp Step Change at t=200ms and Induced Bus Noise of 10 Watts.

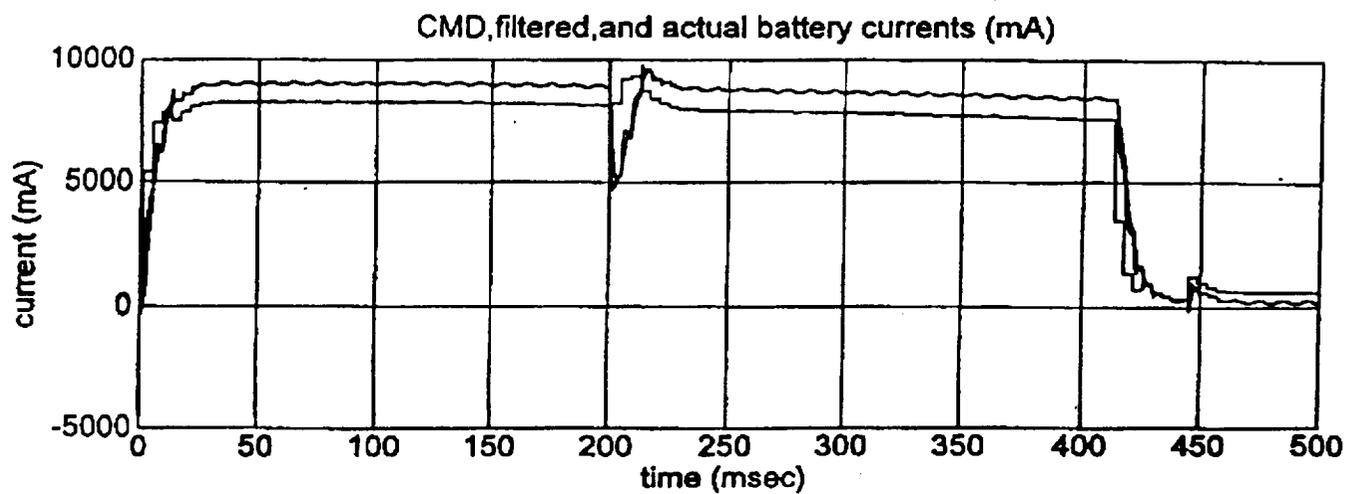
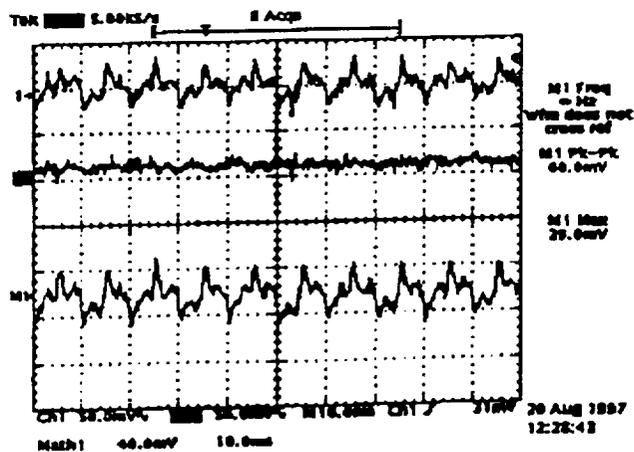


Figure 6: Higher Bandwidth System Response to a 5 Amp Step Change at t=200ms and Induced Bus Noise of 10 Watts.



The algorithm used to compute the control signal to the PWM is dependent on the sampled values of battery current, battery voltage, battery temperature and PWM status. PWM status is the percent duty cycle of the switching FET in analog form. The calculated battery state of charge is also used to determine the charge mode of the battery. It is a proportional controller that will operate on differences between calculated, desired values and measured values of battery current and voltage.

Challenges Presented by Software Control

Some of the challenges introduced by the software controlled system include the quantization of the analog signals, limited software bandwidth and the sampling delays resulting from the analog to digital converter (A/D). The quantization of the analog signals used for the control algorithms caused the PWM drive signal to adjust by discrete levels, thus producing noticeable steps in the signal forming the PWM duty cycle. The effects on the output power bus are minimal, with no noticeable 4msec ripple seen down to the millivolt level. However, the 4msec update rate is detected with a spectrum analyzer, so the modulation is present even as it is not readily detectable in the time domain. One improvement for this was to have the software calculate a proportional change in the bus voltage transient rather than an absolute commanded change, in order to smooth the variation of values of the commanded drive signal.

Limitations of the software bandwidth resulted from the microprocessor operating system and its scheduled tasks supporting spacecraft telemetry. The effect is a less than optimal computation update rate. The processor load, in addition to the delays incurred in the A/D conversion, limit the computation rate, and thus, slow the system response. The 4 ms cycle time did work in the system, although hardware adjustments were needed to avoid a violation of the Nyquist criterion for sampling analog signals. During test, it was shown that a slower update rate did cause the system to overshoot following fast transients. Some modifications to the hardware filters and adjustment of the code algorithm has corrected for the slower than desired computation time. Specifically, the analog signal filter bandwidths were increased, so the algorithm would operate on signals with less delay. We found that the reduced bandwidth filters caused the software drive signal to overcorrect to load transients (Figure 5). When the filter bandwidth increased, the software could better track the changes in load. Figure 6 shows the higher bandwidth system response to a 5 Amp step change in load at 200msec. Also included in the model is the 10 Watt spin rate noise imposed on the bus by the MAP reaction wheels. Both high rate constant current charge and trickle charge are shown, in addition to voltage mode. The amplitude of the bus voltage change subjected to the spin rate noise is less than 25mVp-p

in the model. When measured with the engineering unit, the noise was 30mVp-p, illustrated in Figure 7.

The switching of the analog multiplexer (mux) before an A/D conversion caused a voltage spike at the A/D input. The corrective action was to place the sampled signals of similar magnitude closer to each other in the A/D read cycle. The other fix was to have the software set the mux channel, make other calculations, then return to do the conversion after the voltage spike has subsided.

4. CONCLUSIONS

This paper presents a new generation of satellite power systems that incorporate both analog and digital circuitry for closed loop system control. The generic MIDEK power system design is being tailored to several upcoming space flight missions. The design implements a software outer control loop for flexibility and is the first use of a software controlled power system at Goddard Space Flight Center. The digital control introduces a number of challenges for stability and system response. The hardware and software design is presented and the test results are shown. Future work will include analysis of the stability margins in the various software control modes and further characterization of the system code algorithm for sensitivity to gain and bandwidth changes.

5. REFERENCES

[1] John Ruffa, et al., "MIDEK Advanced Modular and Distributed Spacecraft Avionics Architecture", 1998 *IEEE Aerospace Conference Proceedings*, March 21-28, 1998.

6. BIOGRAPHY

Karen Castell is an Electrical Engineer with the Space Power Applications Branch at Goddard Space Flight Center in Greenbelt, MD. She holds a patent on a low noise, high voltage power supply design that is successfully operating on the Proportional Counter Array (PCA) instrument on the X-ray Timing Explorer (XTE) spacecraft. She presently supports the MAP spacecraft as the Power System Lead Engineer. Karen earned her BSEE from Duke University and her MSEE from Northeastern University.

Amri Hernandez-Pellerano is an Electrical Engineer in the Space Power Applications Branch at Goddard Space Flight Center, Greenbelt, MD. She was previously part of the Power System Electronics team for the Tropical Rainfall Measuring Mission (TRMM), which was developed in-house at GSFC and is scheduled to launch from Japan in

November of 1997. She currently works on the Microwave Anisotropy Probe (an in-house spacecraft development program at GSFC) as the Power System Electronics Lead as well as one of the designers. She has a BSEE from the University of Puerto Rico at Mayaguez Campus and a MSEE from the Johns Hopkins University.

Margaret Wismer is an assistant Professor of Electrical Engineering at Bucknell University. She teaches courses in electric power, instrumentation and electronics. Her research interests include electric power systems, power supplies, controls and system modelling. She came to Bucknell from Worcester Polytechnic Institute where she received her Ph.D and MSEE. She has a BSEE from Carnegie Mellon.

7. APPENDIX A

Development of the Solar Array Pulse Width Modulator Hardware Design

In an effort to reduce the size and cost of the hardware, while also maintaining low output ripple, the solar array pulse width modulator design was analyzed and optimized. Several designs were considered for the input filter compensation network. Among them was a simple, passive network across each filter component, an active filter design in the power stage and a dV/dt network that feeds into the duty cycle of the power switch. The role of the input filter compensator is to damp the oscillations of the input voltage across the regulated solar array. This voltage can have a large ripple due to the switching within the regulator. A model of the PWM circuit was developed in order to complement the hardware design and testing. A more detailed picture of the regulator circuit is shown in Figure 8. Switch S1, represents the switching FET that is controlled by a 125 kHz pulse width modulated (PWM) signal. The input inductance, L_i and capacitance, C_i , are required to filter the input voltage, V_i . The output capacitor, C_o , filters the output current, I_o . This type of switchmode regulator is also referred to as a boost converter since the output voltage, V_o , is higher than V_i .

As shown in Figure 2, the desired battery current is automatically fed to the inner control loop which regulates the %D of the PWM converter circuit. This inner control loop actually consists of three embedded negative feedback loops. The three variables controlled by these feedback loops are V_i , I_o , and the battery current, I_{bat} . These loop filters and gain circuits are implemented with operational amplifier circuits. System stability and circuit modeling of these control loops are considered in the following sections.

Details of the Hardware model

The purpose of the system modeling is to easily assess stability, explain unexpected behavior and evaluate possible modifications and enhancements for future designs. The power stage is modeled with the solar arrays and battery connected to the power bus with the bus capacitance, C_{bus} , line inductance, L_{line} , and C_i , L_i and C_o in the converter. (See Figs. 8 and 9.) A system of state-space averaged differential equations is written to simulate the time evolution of system variables such as V_i , V_o , V_{load} and I_o . The state-space averaging technique requires that any transients on the system be much slower than the switching period in the converter circuit. The PWM signal controlling the state of switches S1 and S2 can then be represented by the %D which is a continuous time signal. To obtain the system model, a first order state-space equation is written for each energy storage element in the power circuit. These equations, which are typically nonlinear, can be linearized if

one wishes to investigate the gain and phase margins of the feedback loops.

The feedback network of the power system is modeled with its active analog and digital circuits. The analog part is implemented with op-amp filters whose cutoff frequencies are chosen to ensure stability with a quick response. These linear filters can be modeled easily by their transfer functions in the Laplace or complex frequency domain. The digital logic is implemented in software. The code is written in C++ on an R000 microprocessor with 32k of memory. The software contains the algorithm used to update the battery current as well as logic functions that control the state of the solar array shunts.

These equations, the digital logic, the analog transfer functions and the state-space equations for the power bus can be incorporated into a composite model with MatLab/Simulink(r). Time response plots of either state or control variables can be easily obtained to assess the impact due to load changes. A typical MatLab diagram of the power bus and system electronics is shown in Figure 11. The power bus system has five inputs which are: the current corresponding to the unshunted solar arrays (where n_s equals the number of unshunted arrays), the duty cycle, the total load current I_{LOAD} , the battery voltage and the 5A current source representing the three solar arrays used in the regulator circuit. The three control outputs are the battery current, I_{bat} , regulator output current, I_o , and the input voltage across the regulator, V_i . The feedback transfer functions, the summing circuits and the digital logic block model some of the functions of the PSE. Choosing the transfer functions such that the system operates within specifications is addressed in the following section.

Hardware Stability Analysis and Control

In order to meet the ripple specifications of 0.5Vp-p on the bus voltage, a second order filter is required at the input of the boost converter. This filter is the series-parallel combination of L_i , C_i and R_i in Figure 9. Without the capacitor, C_i , the input filter is first order with a cutoff frequency equal to R_i/L_i . Since R_i is the input resistance of a current source, L_i would need to be very large in order to effectively reduce the ripple in V_i . Therefore C_i is added to lower the input impedance and thus the cutoff frequency of the input filter. While the resulting circuit filters the 125kHz ripple current, it also causes oscillations of V_i at the $L_i C_i$ resonant frequency. The amplitude of these oscillations will depend on the input current and the average duty cycle of the switch S1. For low duty cycles and a 5A current source, V_i will oscillate by as much as 40Vp-p. Since the output voltage, V_o , is clamped by the battery and the bus capacitance, C_{bus} , these oscillations will not affect the bus voltage transients but will instead cause larger

ripples of the output current, I_o . It is desirable therefore to implement a design which eliminates these oscillations while meeting all other transient specifications for load changes as given in Table 1.

Two possible control loop designs are investigated and compared for response time and voltage oscillation. One method is to feed back the derivative of the input voltage to the duty cycle. This is equivalent to adding a phase lead compensator in the input voltage loop. This feedback signal is referred to as dV_i/dt . A simple block diagram showing this loop implementation is shown in Figure 12. Bode plots of V_i/V_c , for which V_c is the control voltage, and the dV_i/dt transfer functions are shown in Figures 13a and 13b. The "cut-in" frequency, f_c , in Figure 13b is controlled by the product of R_{34} and C_{24} . If f_c is set too low, the response time of V_i will be relatively slow but if f_c is too high, V_i will oscillate more and the system will be unstable. The cut-in frequency was chosen to be 1.6kHz which is low enough to damp the L_iC_i oscillations. The Bode plot in Figure 13c shows the open loop transfer function and can be obtained by adding together the plots of Figs. 13a and 13b. This plot shows a gain and phase margin which indicate that the closed loop response will be unconditionally stable.

A second loop can now be added to control the regulator output current I_o as shown in Figure 14. The feedback transfer functions are chosen such that the low frequency gain is high and the high frequency gain is low and rolls off quickly. This will ensure that the system has a fast response time while rejecting additive white noise due to sensors or external sources.

A potential problem with this controller could arise with load changes of 5A or more. An increase of 5A load is used to model the microwave radiometer turning on, while a decrease in 5A simulates turn off. Since the supply for the fine-tuning regulator is 5A, the circuit will go into the nonlinear region with a 5A transient load. Thus when the load decreases by 5A, the output of the regulator should go to 0A implying that $\%D$ will also be zero. This means switch S_1 in Figure 9 will appear as a short forcing the input voltage to oscillate at the resonant frequency of the L_iC_i circuit. These oscillations will continue until the software sends a signal to open one of the solar array shunts, or n_s in Figure 11 is increased by 1. As the $\%D$ goes above zero the dv/dt filter will again operate in the linear region and the oscillations will decay.

Eliminating the input voltage oscillations can also be accomplished by using a higher order passive filter across the switch. These "snubbing" circuits, used in lieu of the dv/dt loop, are an RC series circuit connected across C_i and RL combination across L_i in Figure 9. The time constants are chosen to be relatively long such that neither C_i nor L_i can be fully charged to the peak value of the oscillation voltage. Effectively the cutoff frequency is far below the resonant frequency and therefore only the DC value of V_i is seen at the input. The open-loop system will therefore be stable obviating the need for a phase-lead controller. This type of compensation was chosen for the MAP design for its simplicity and robustness.

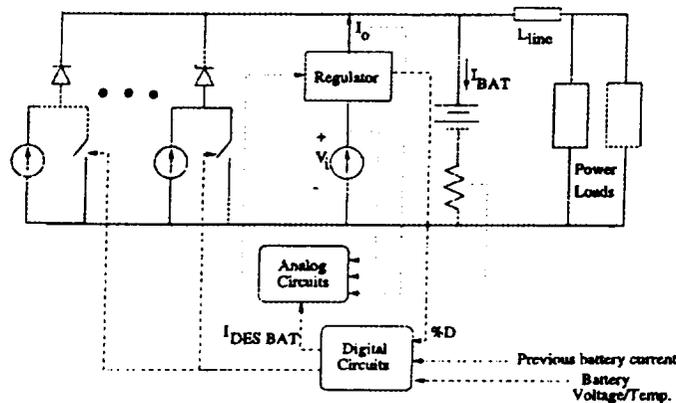


Figure 8: Simplified Schematic of the MIDEX Power System showing the solar array, battery and PSE control signals.

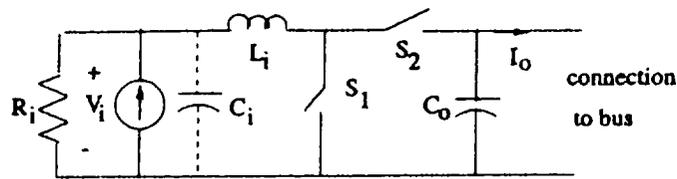


Figure 9: Switchmode regulator used for fine tuning the bus current.

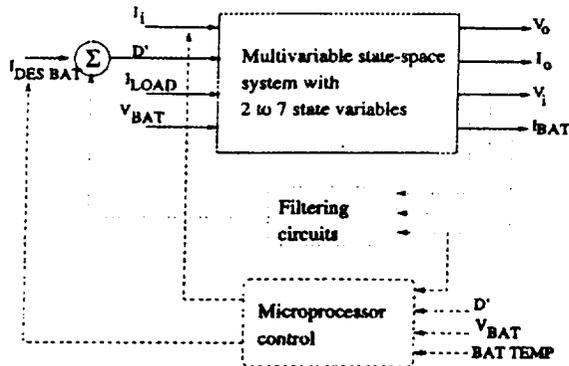


Figure 10: State space model of the feedback control loop

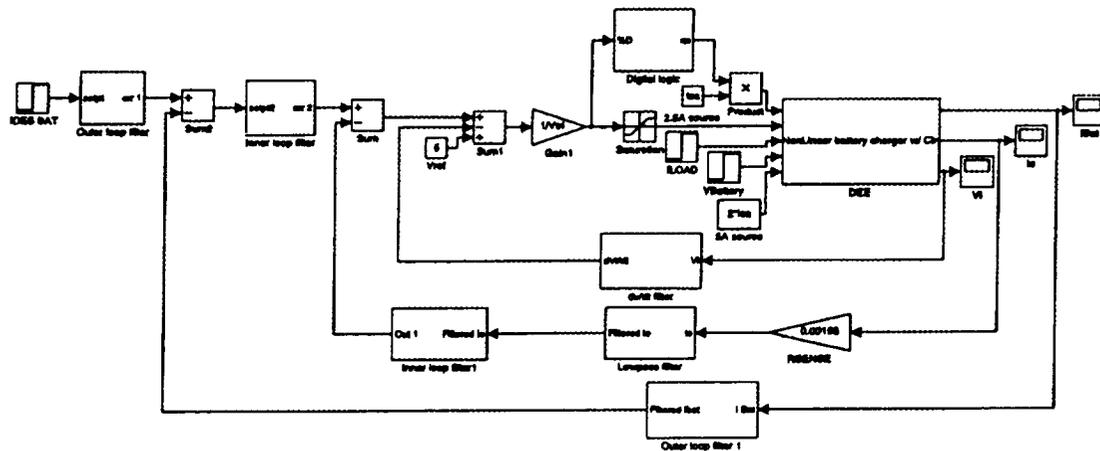


Figure 11: MatLab Simulation of the PSE filtering and logic functions.

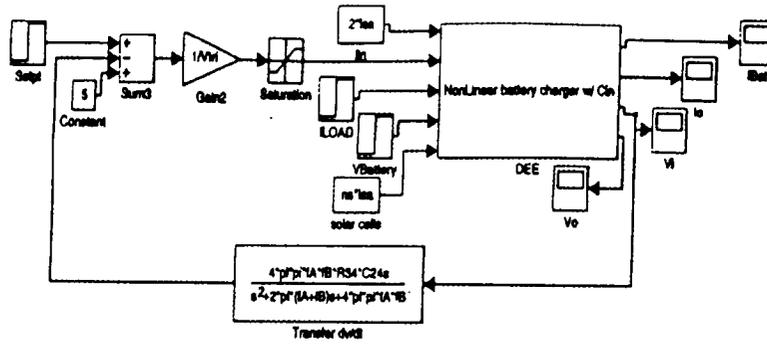


Figure 12: Model of the phase-lead compensator added to filter the input voltage, V_i .

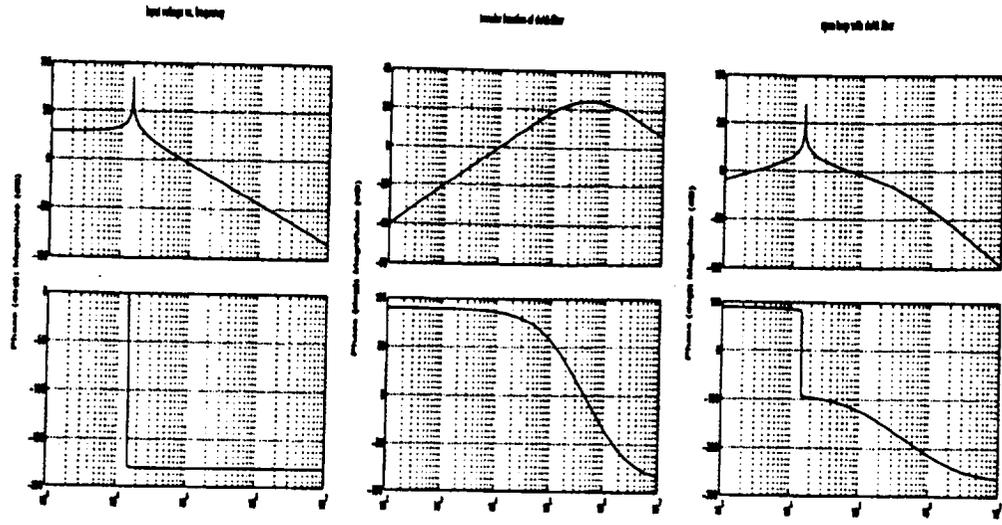


Figure 13: Gain and phase plots of a) V_i vs. frequency of the uncompensated system, b) the dV_i/dt filter and c) V_i vs. frequency of the compensated system.

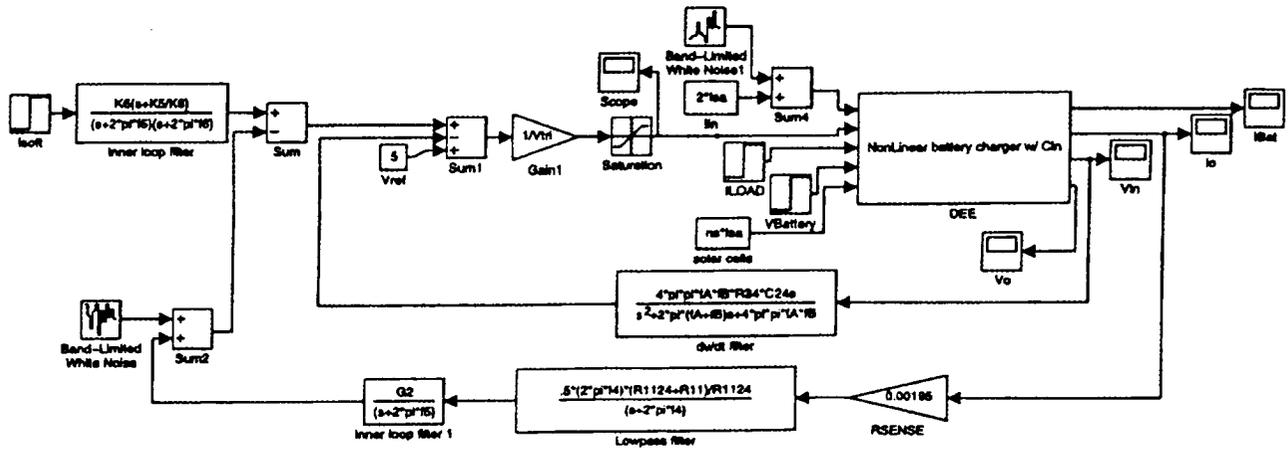


Figure 14: Model of the phase-lag compensator for regulator current, I_o , control.